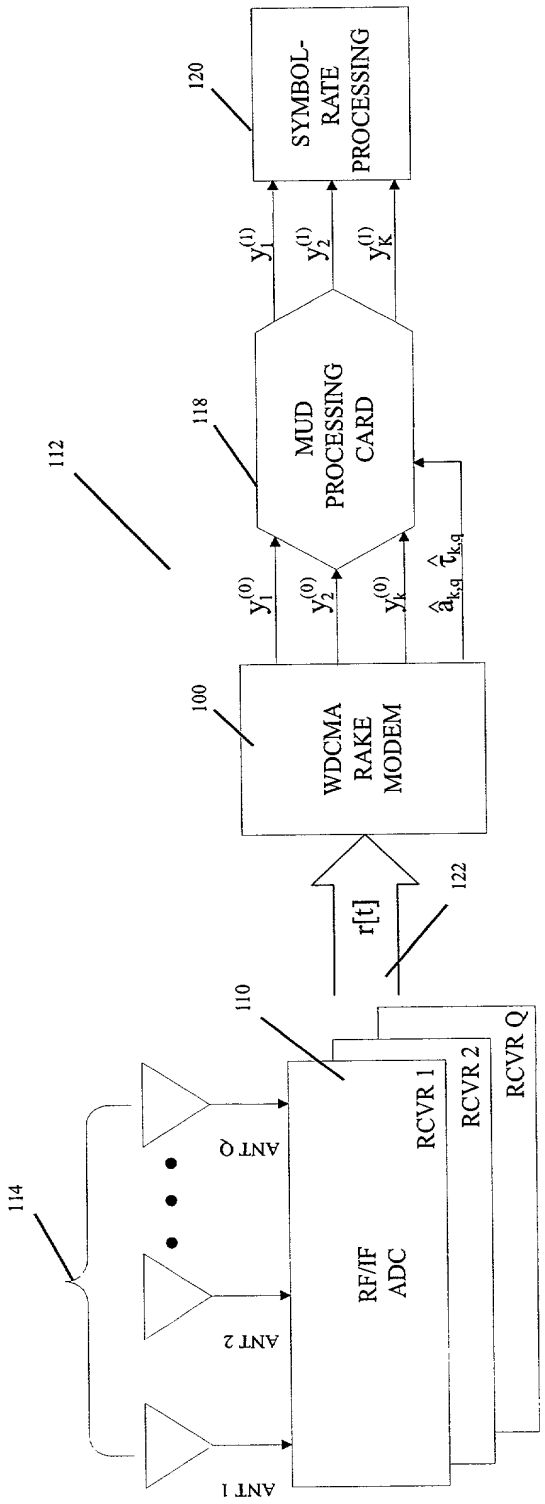

ANT 1
ANT 2
ANT Q
114
RF/IF
ADC
RCVR 1
RCVR 2
RCVR Q
110
r[t]
122
WDCMA
RAKE
MODEM
100
$y_1^{(0)}$
$y_2^{(0)}$
$y_K^{(0)}$
$\hat{a}_{k,q}$
$\hat{\tau}_{k,q}$
112
MUD
PROCESSING
CARD
118
$y_1^{(1)}$
$y_2^{(1)}$
$y_K^{(1)}$
SYMBOL-
RATE
PROCESSING
120

Figure 1

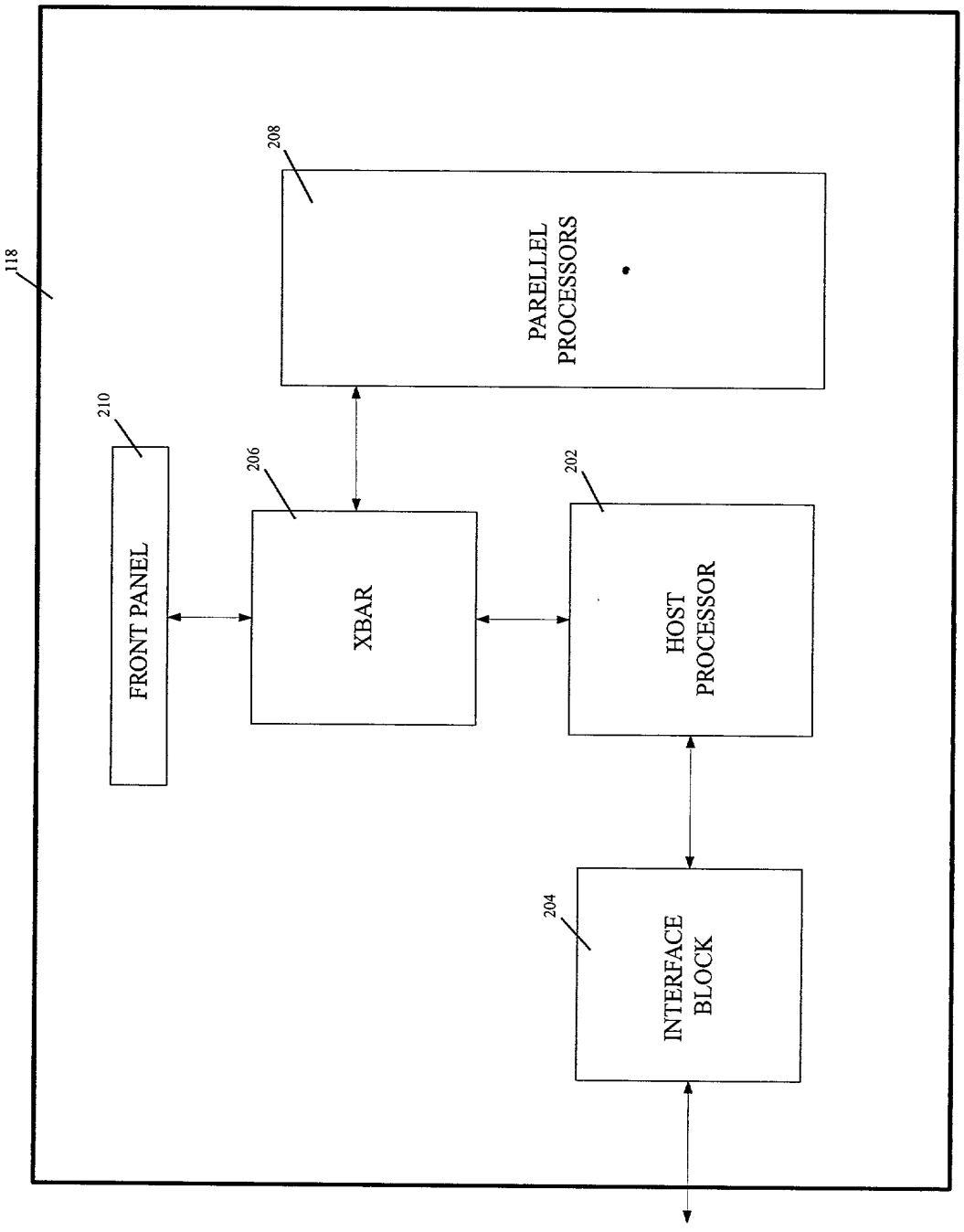

118
208
PARELLEL PROCESSORS
210
206
202
FRONT PANEL
XBAR
HOST PROCESSOR
204
INTERFACE BLOCK

Figure 2

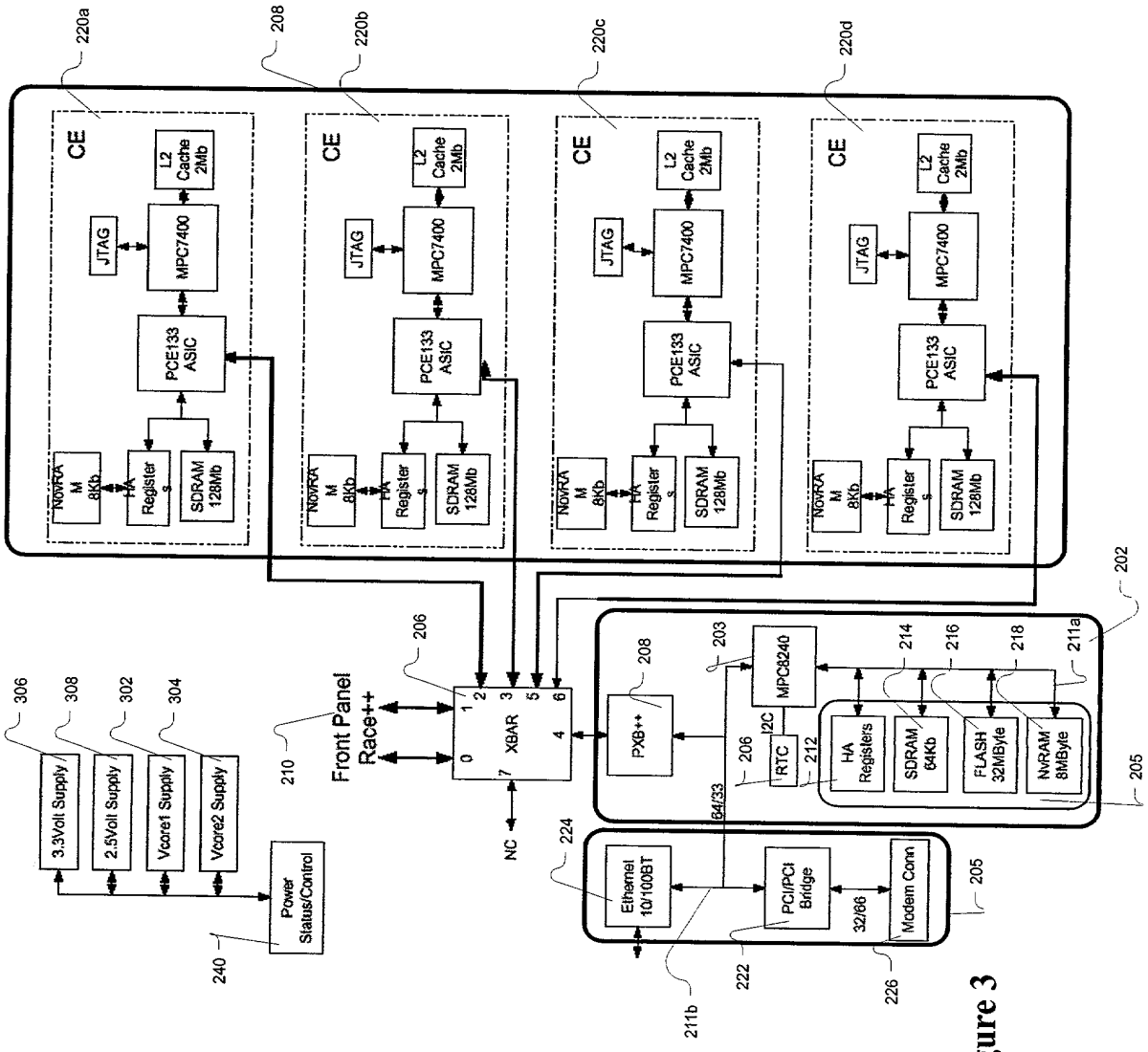

220a
208
220b
220c
220d
CE
L2 Cache 2Mb
JTAG
MPC7400
PCE133 ASIC
NovRA M 8Kb
HA Registers
SDRAM 128Mb
206
Front Panel Race++
210
XBAR
0
1
2
3
4
5
6
7
NC
202
PXB++
208
203
MPC8240
I2C
RTC
212
214
216
218
211a
HA Registers
SDRAM 64Kb
FLASH 32MByte
NvRAM 8MByte
205
64/33
224
Ethernet 10/100BT
PCI/PCI Bridge
32/66
Modem Conn
205
211b
222
226
306
308
302
304
3.3Volt Supply
2.5Volt Supply
Vcore1 Supply
Vcore2 Supply
Power Status/Control
240

Figure 3

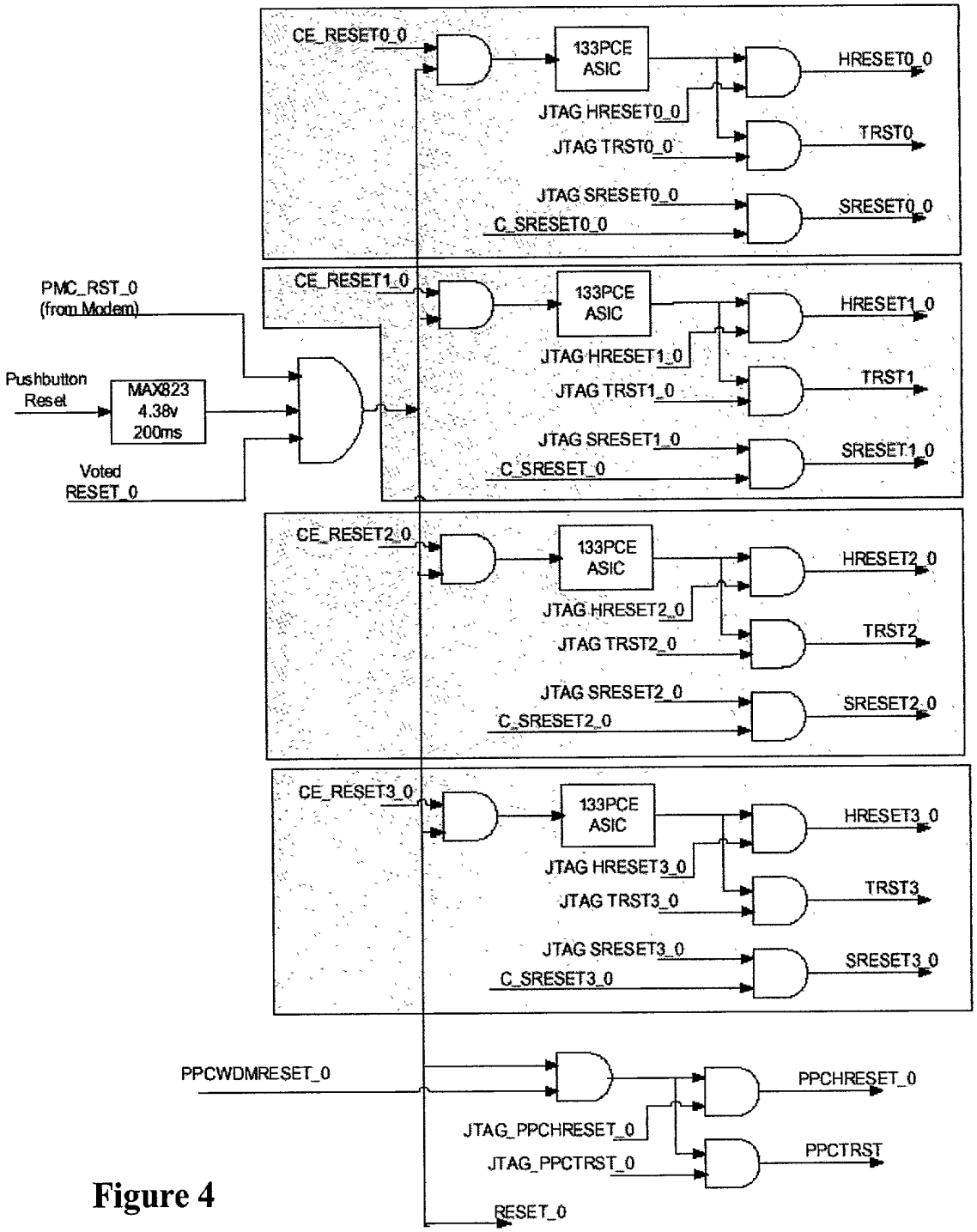

CE_RESET0_0
133PCE ASIC
HRESET0_0
JTAG HRESET0_0
TRST0
JTAG TRST0_0
JTAG SRESET0_0
SRESET0_0
C_SRESET0_0
CE_RESET1_0
PMC_RST_0 (from Modem)
133PCE ASIC
HRESET1_0
JTAG HRESET1_0
Pushbutton Reset
MAX823 4.38v 200ms
TRST1
JTAG TRST1_0
JTAG SRESET1_0
SRESET1_0
Voted RESET_0
C_SRESET_0
CE_RESET2_0
133PCE ASIC
HRESET2_0
JTAG HRESET2_0
TRST2
JTAG TRST2_0
JTAG SRESET2_0
SRESET2_0
C_SRESET2_0
CE_RESET3_0
133PCE ASIC
HRESET3_0
JTAG HRESET3_0
TRST3
JTAG TRST3_0
JTAG SRESET3_0
SRESET3_0
C_SRESET3_0
PPCWDMRESET_0
PPCHRESET_0
JTAG_PPCHRESET_0
PPCTRST
JTAG_PPCTRST_0
RESET_0

Figure 4

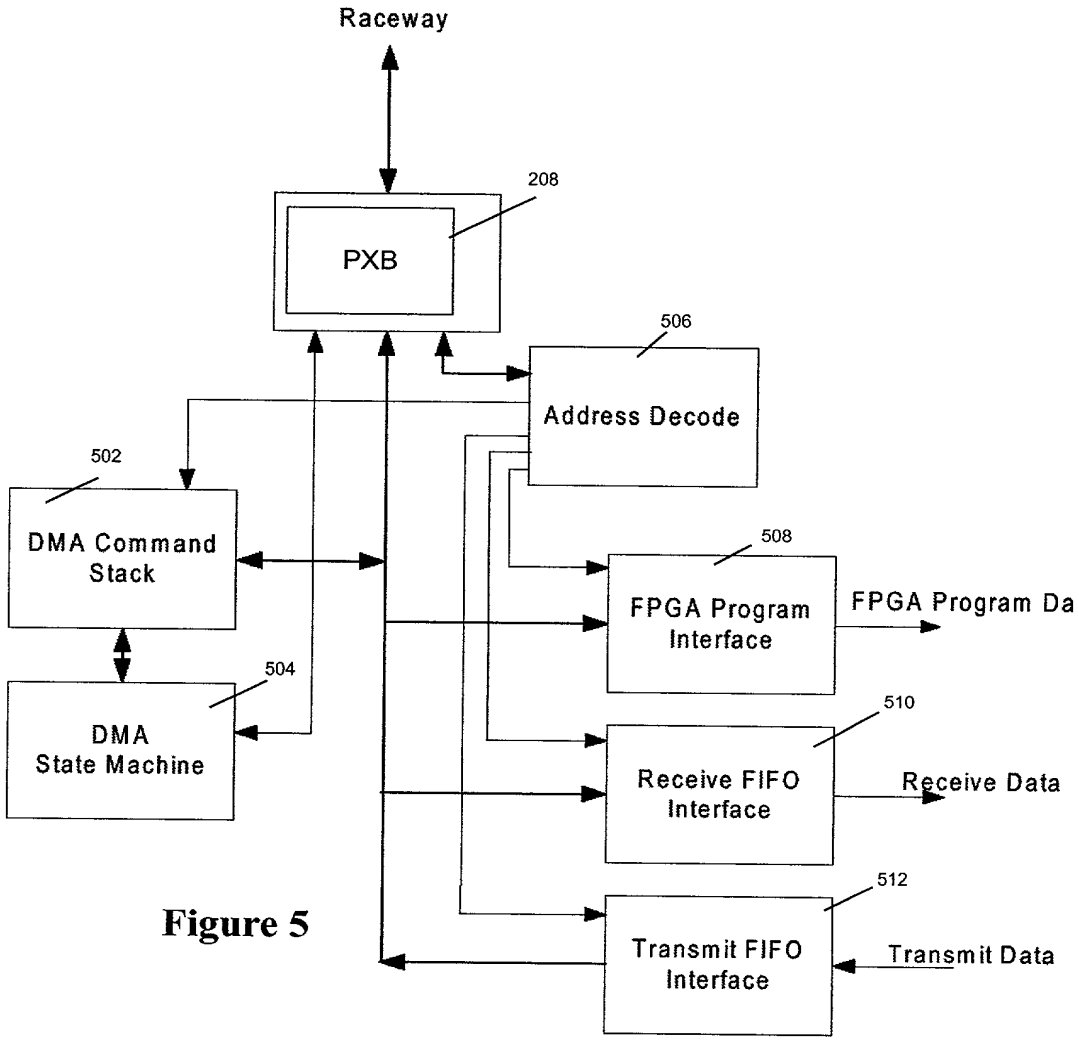

Raceway
208
PXB
506
Address Decode
502
DMA Command Stack
508
FPGA Program Interface
FPGA Program Da
504
DMA State Machine
510
Receive FIFO Interface
Receive Data
512
Transmit FIFO Interface
Transmit Data

Figure 5

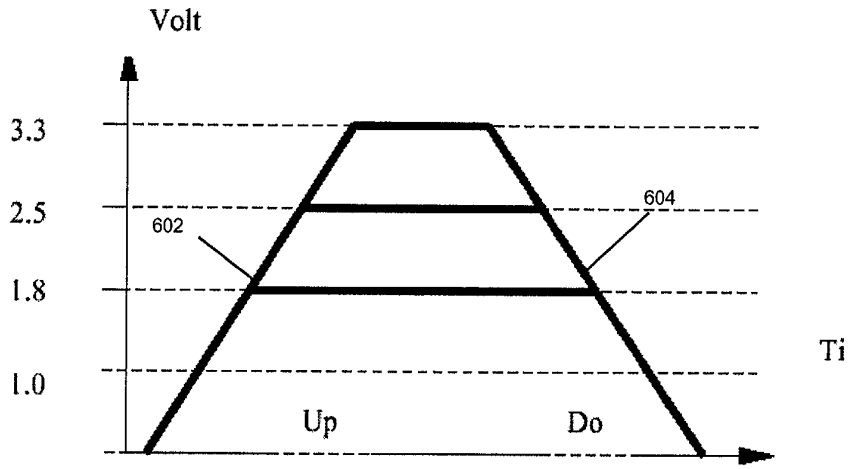
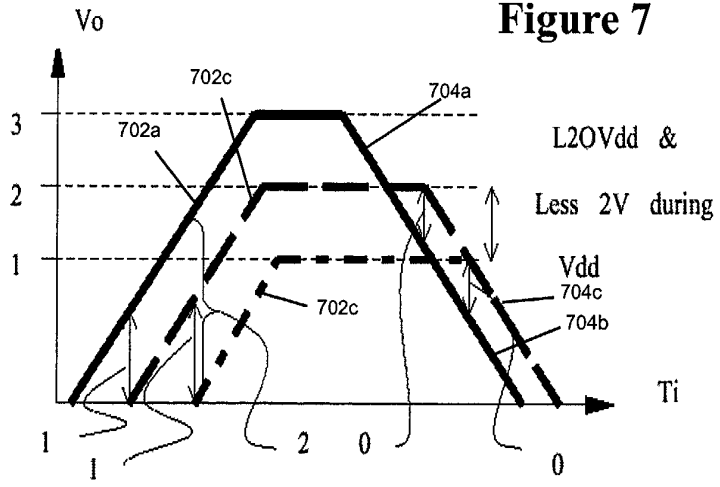


Figure 6

Figure 7



Express Mail Label: US EV 093 931 797 US

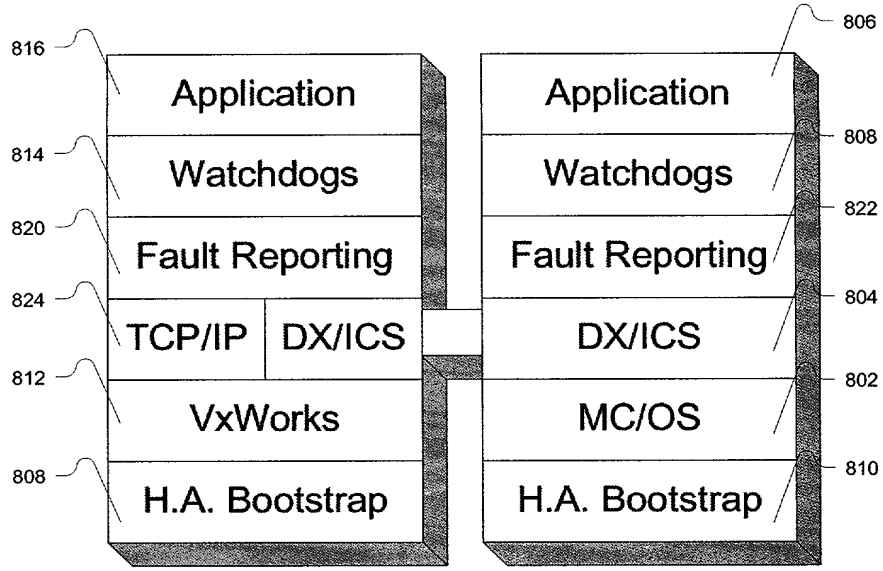


Figure 8

Host 8240

Compute Elements

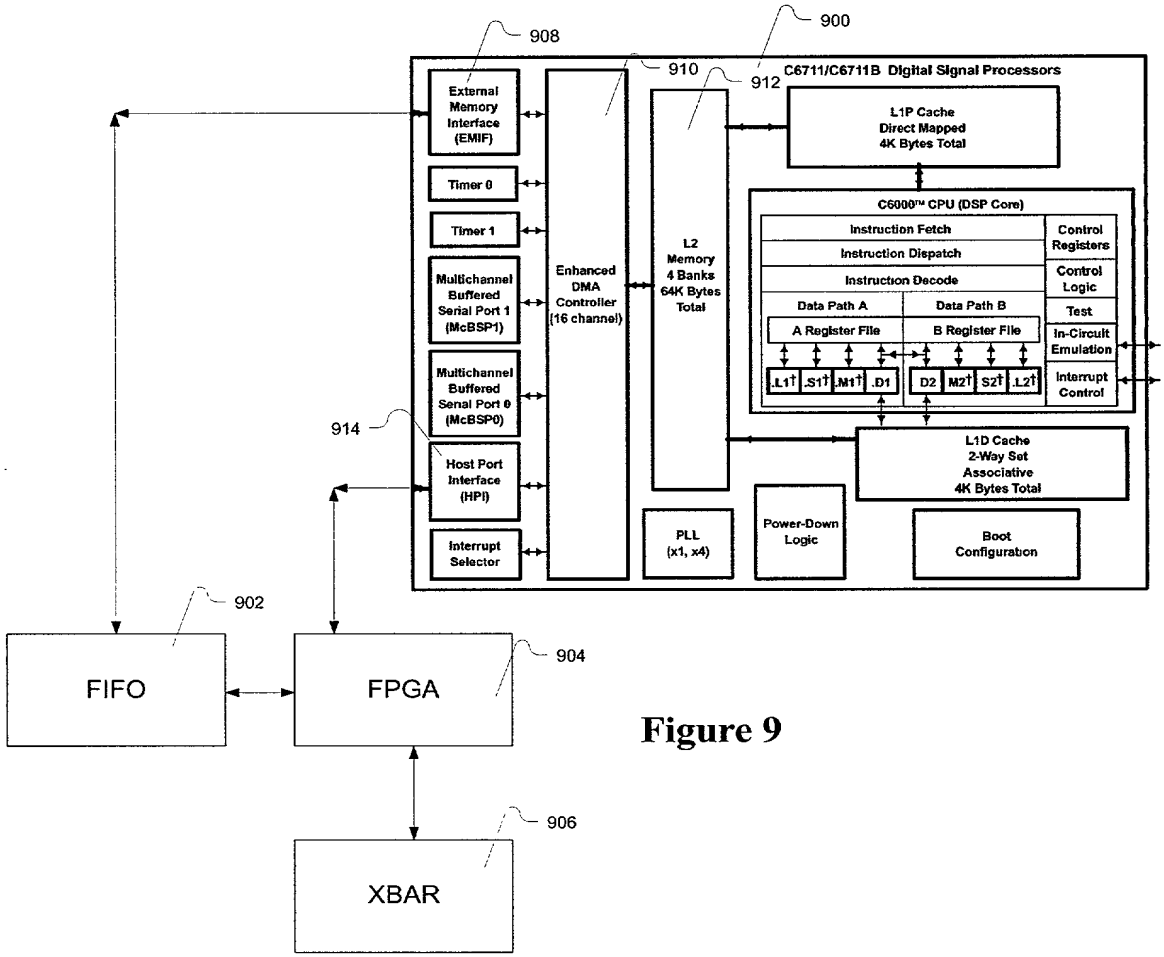


Figure 9

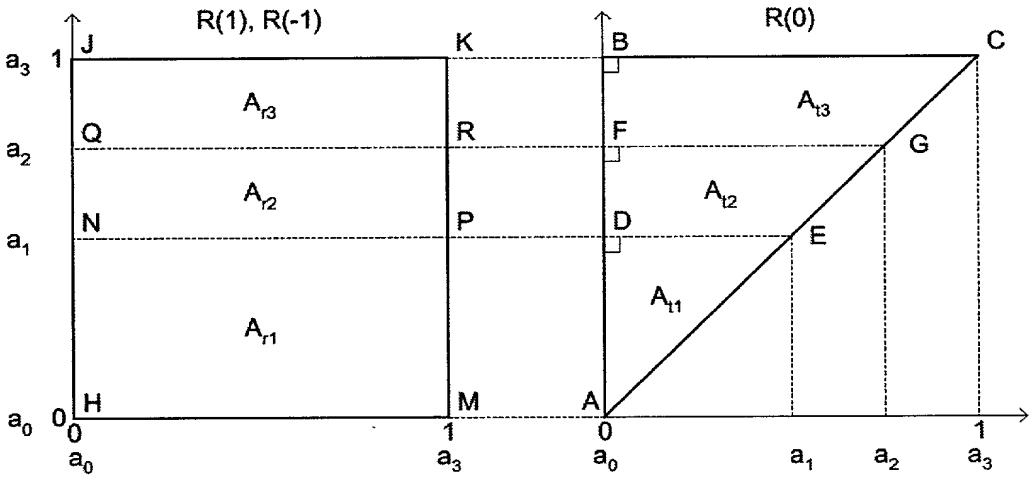


Figure 10

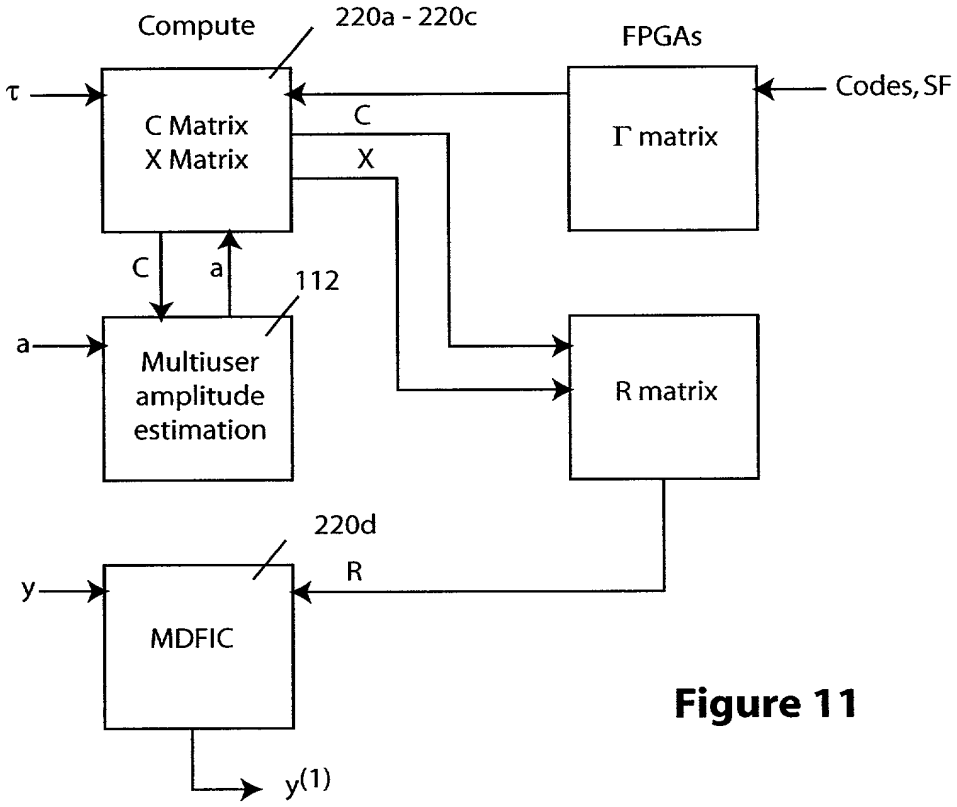


Figure 11

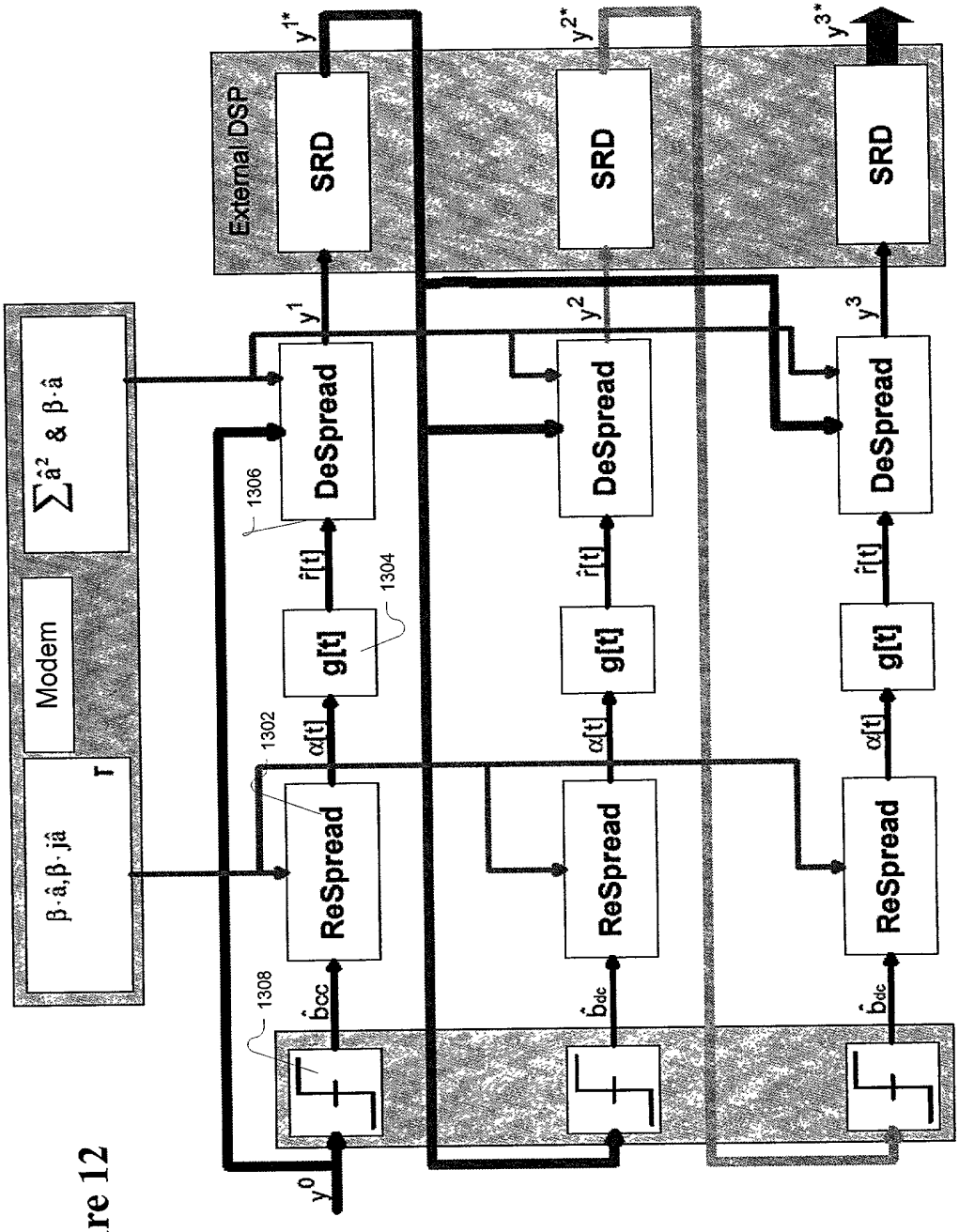

External DSP
SRD
SRD
SRD
y^{1*}
y^{2*}
y^{3*}
y^1
y^2
y^3
y^0
DeSpread
DeSpread
DeSpread
1306
r[t]
g[t]
1304
1302
α[t]
ReSpread
ReSpread
ReSpread
1308
$\hat{b}_{cc}$
$\hat{b}_{dc}$
$\hat{b}_{dc}$
$\sum \hat{a}^2$ & $\beta \cdot \hat{a}$
Modem
$\beta \cdot \hat{a}, \beta \cdot j\hat{a}$
r

Figure 12

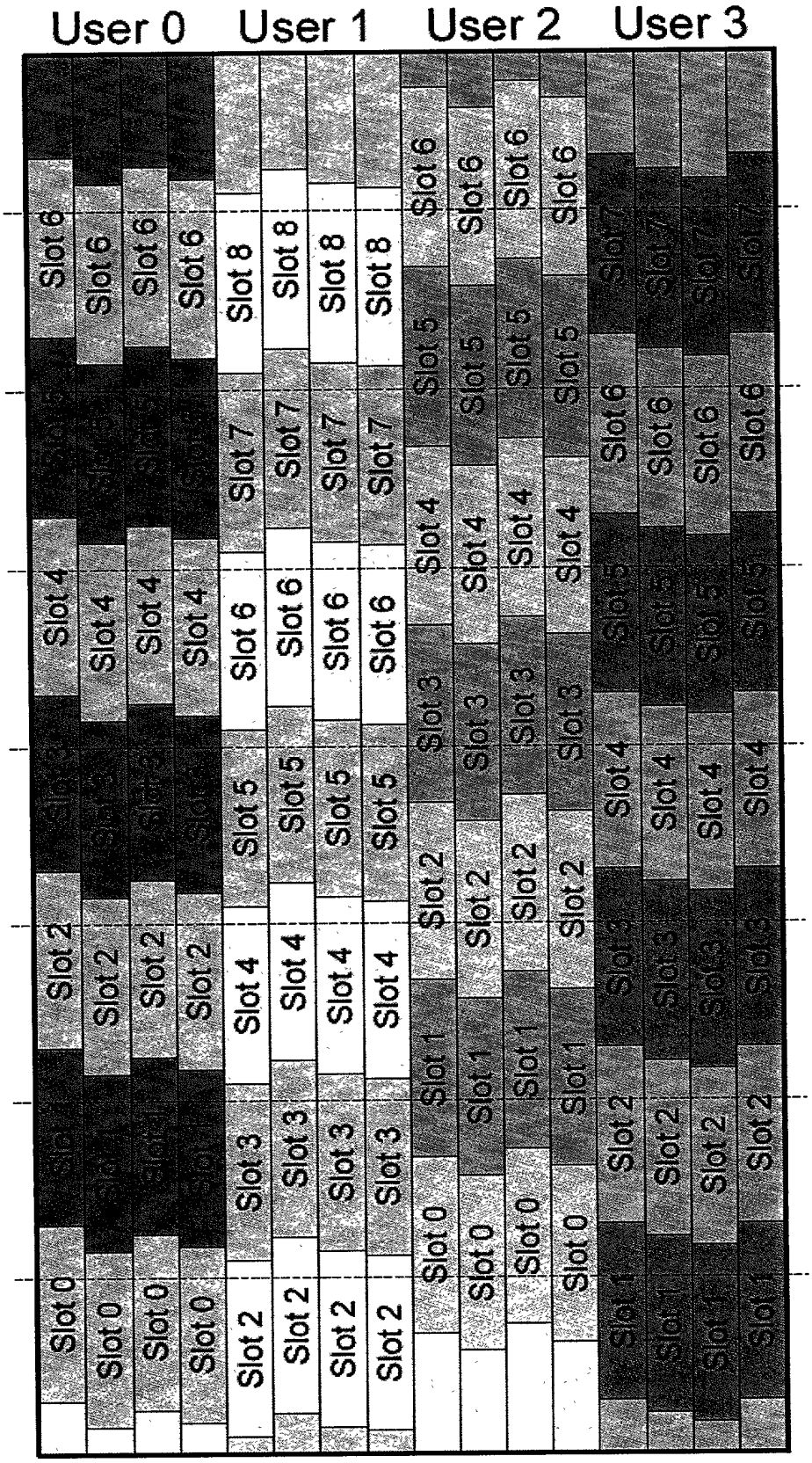

User 0
User 1
User 2
User 3
Slot 0
Slot 1
Slot 2
Slot 3
Slot 4
Slot 5
Slot 6
Slot 7
Slot 8

Figure 13

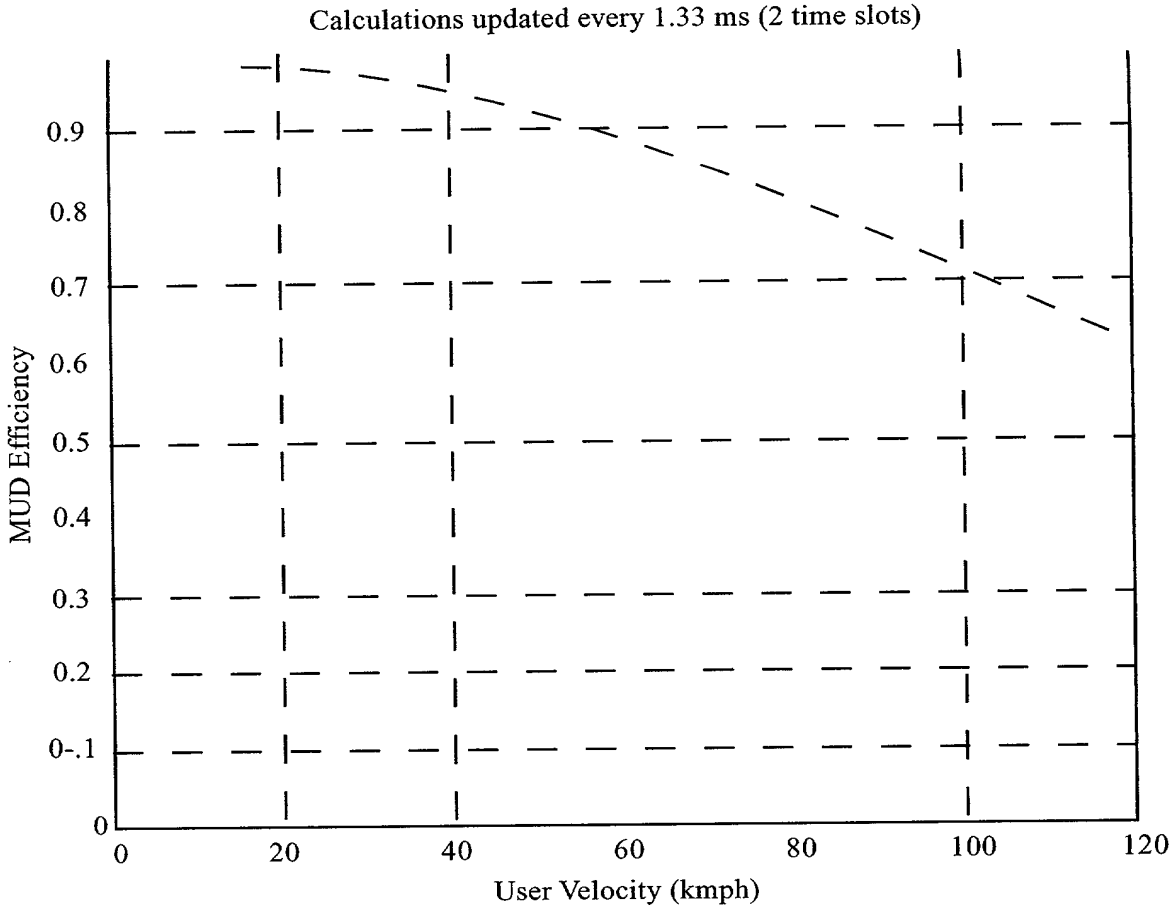


Figure 14

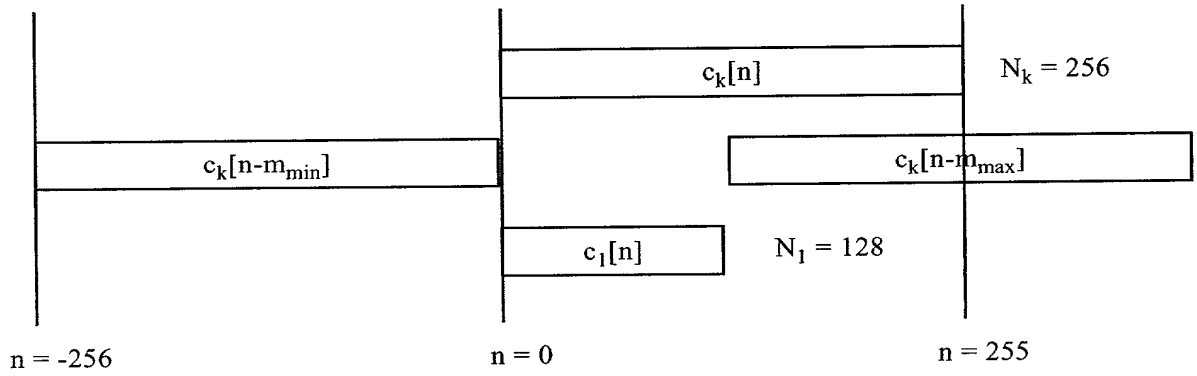


Figure 15

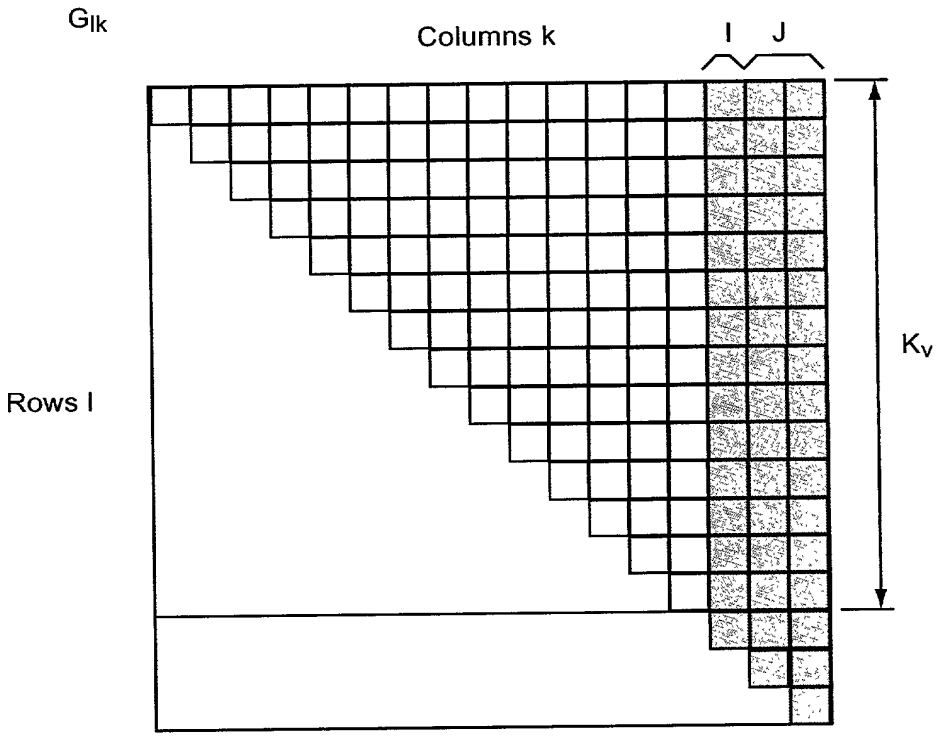


Figure 16

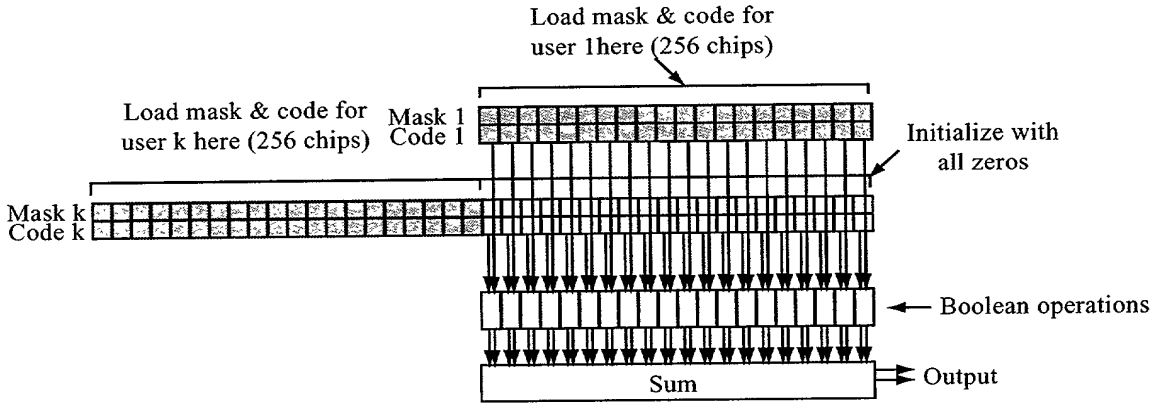


Figure 17

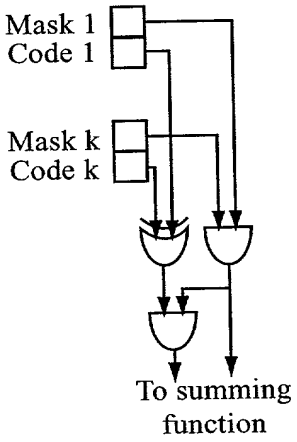


Figure 18

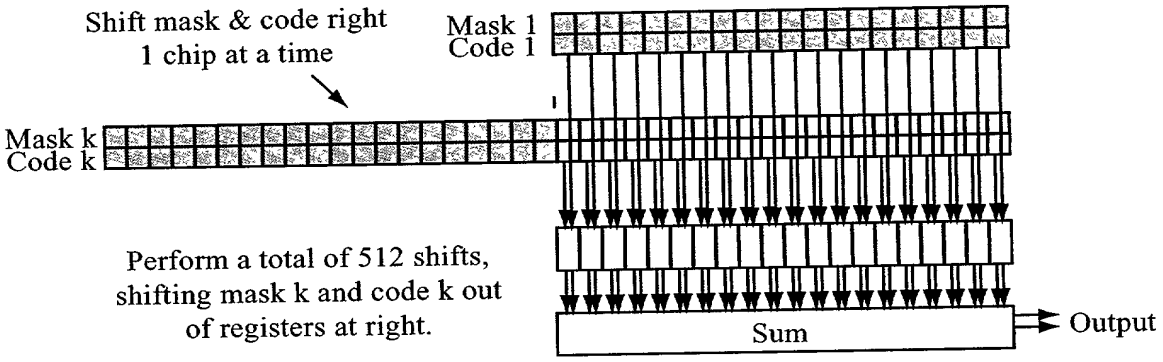


Figure 19

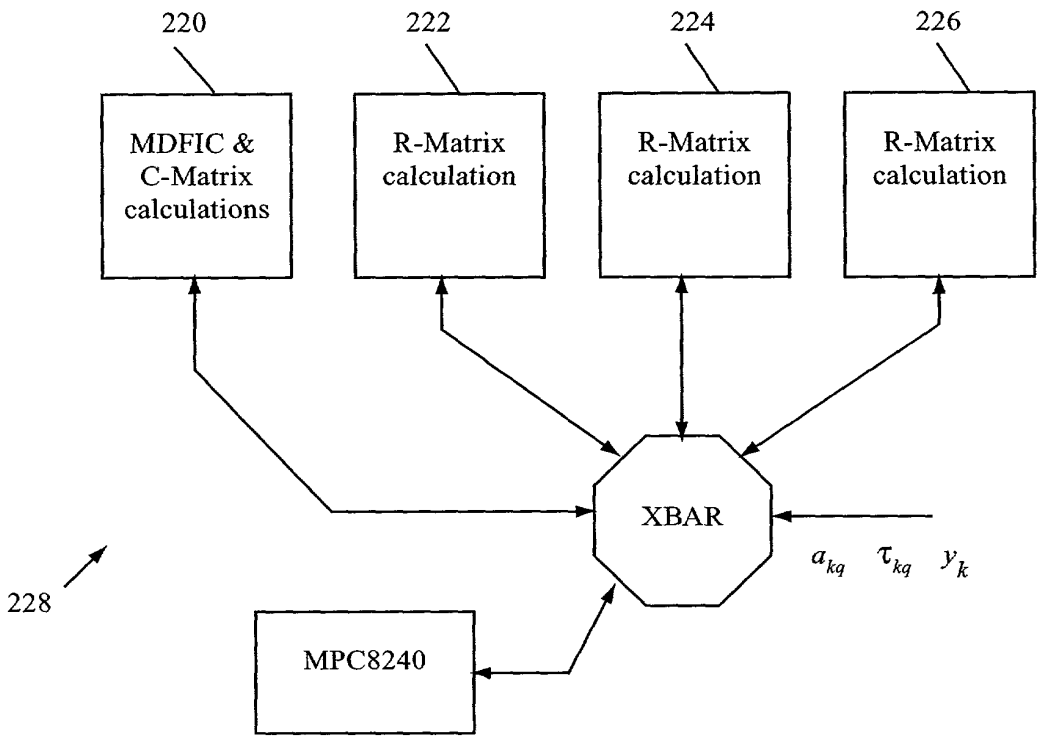

220
222
224
226
MDFIC & C-Matrix calculations
R-Matrix calculation
R-Matrix calculation
R-Matrix calculation
XBAR
a_{kq} τ_{kq} y_k
228
MPC8240

Figure 20

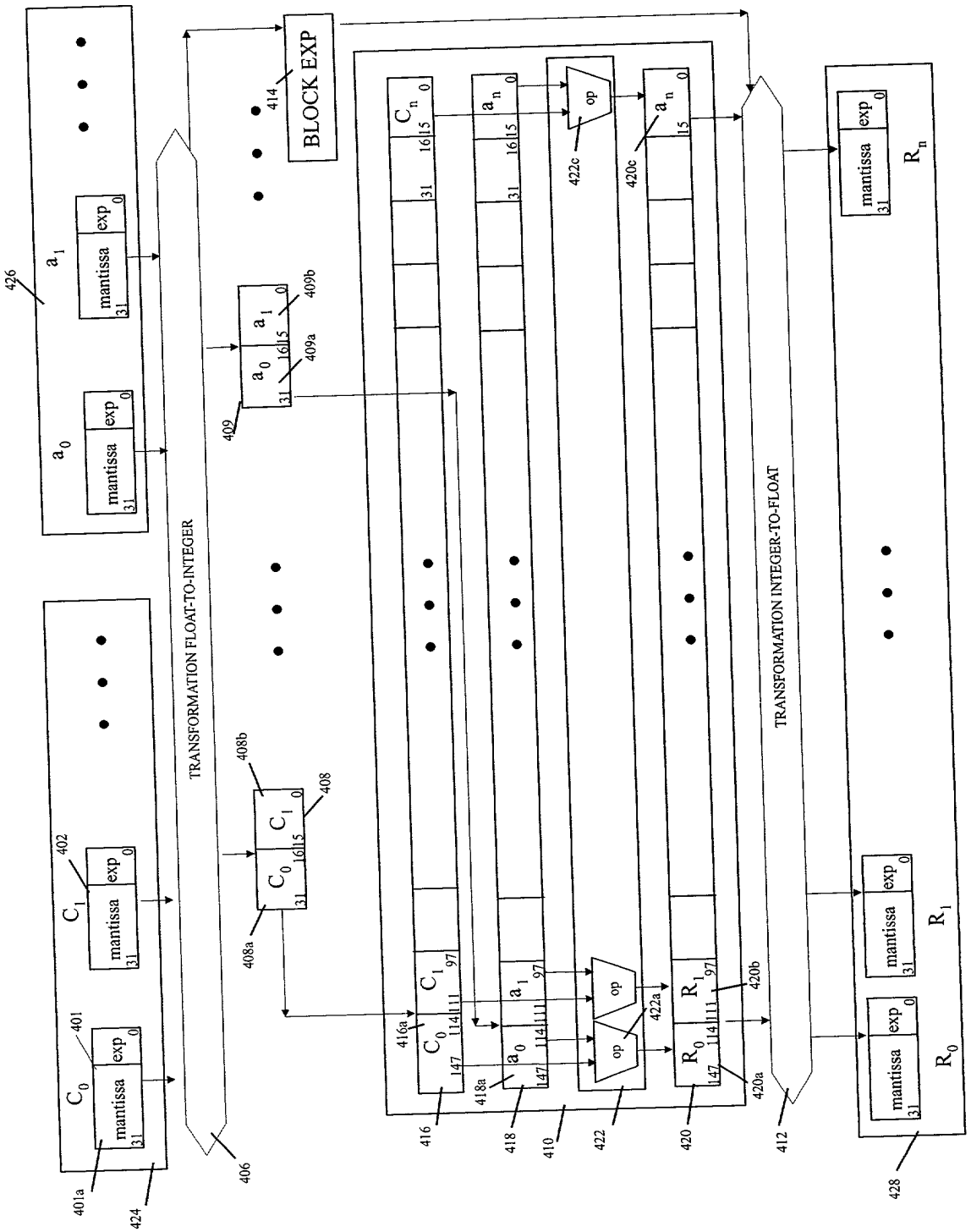

TRANSFORMATION FLOAT-TO-INTEGER
BLOCK EXP
TRANSFORMATION INTEGER-TO-FLOAT
mantissa
exp
op

Figure 21